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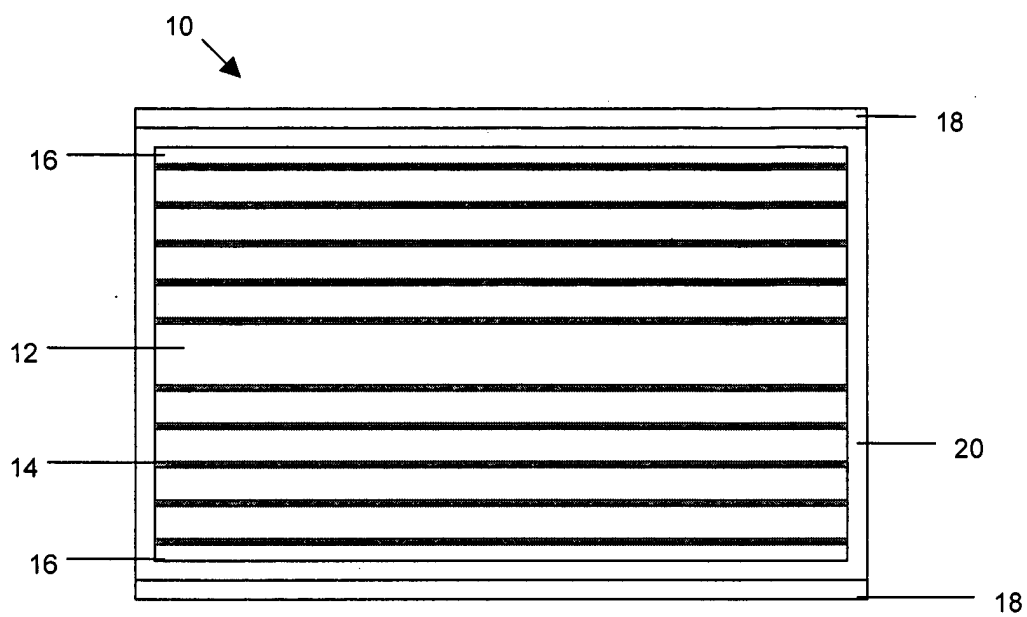


FIG. 1

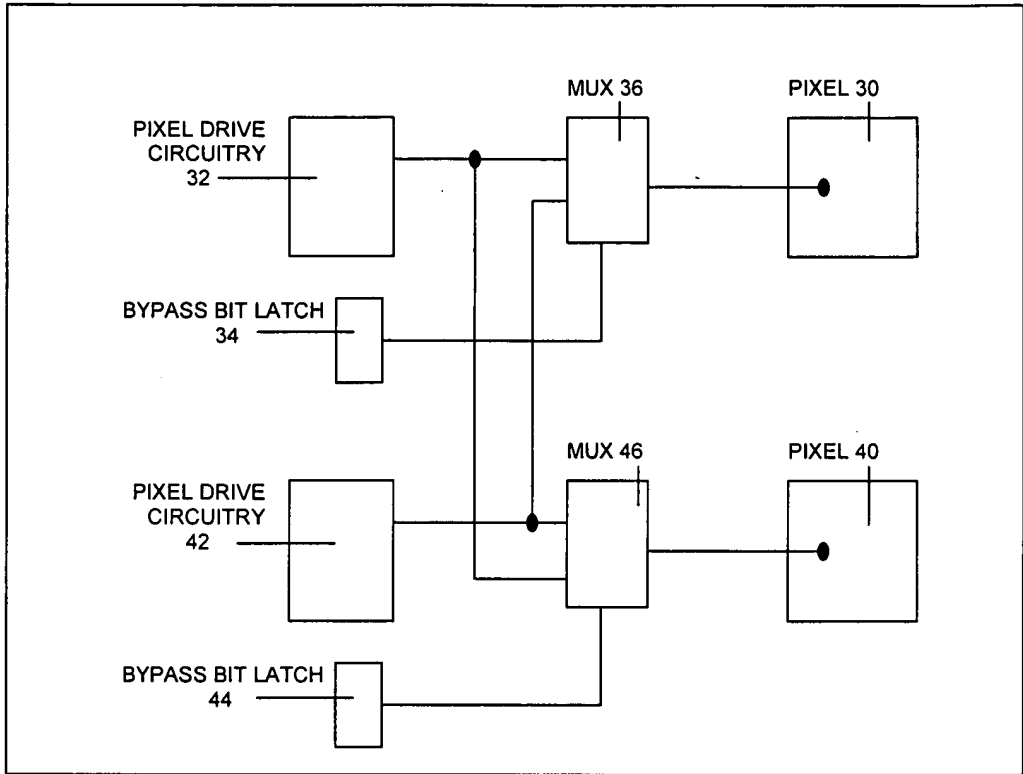
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FIG. 2

The diagram illustrates a pixel driver circuit for two pixels, 30 and 40. A common vertical bus, represented by a zigzag line and labeled R 50, connects the two pixels. Each pixel is connected to this bus through a dot. The bus is driven by two tri-state buffers, 38 and 48. The input of tri-state buffer 38 is connected to a pixel drive circuitry block 32 and a bypass bit latch block 34. Similarly, the input of tri-state buffer 48 is connected to a pixel drive circuitry block 42 and a bypass bit latch block 44. The output of each tri-state buffer is connected to the common bus. The bypass bit latches (34 and 44) are shown as small rectangles with a single input line. The pixel drive circuitry blocks (32 and 42) are shown as larger rectangles with a single input line. The tri-state buffers (38 and 48) are shown as triangles with a control input (small circle) and an output (triangle pointing right).

FIG. 3

VIA CUT BY LASER TO DISCONNECT PIXEL FROM DEFECTIVE DRIVE CIRCUIT

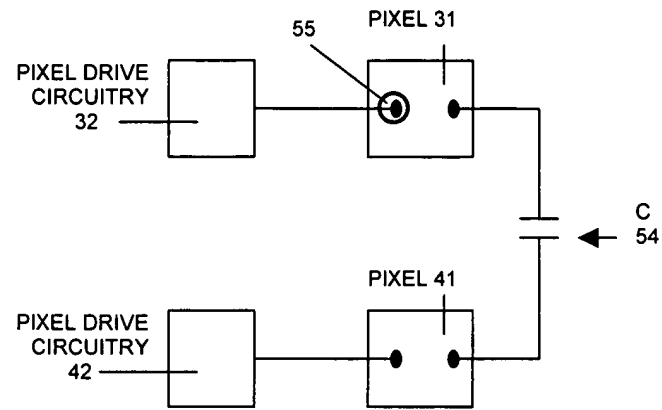
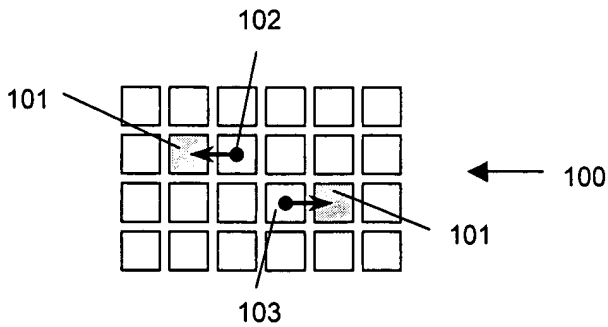


FIG. 5

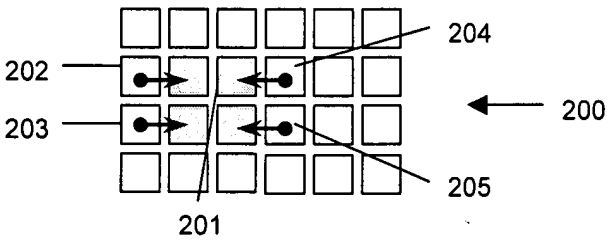
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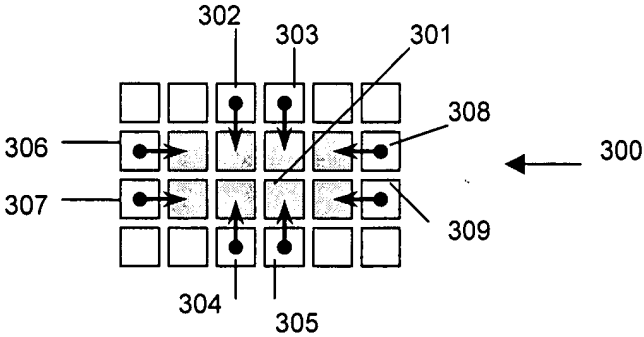
SINGLE-PIXEL (1 X 1).



4-PIXEL GROUP (2 X 2).



8-PIXEL GROUP (4 X 2).



16-PIXEL GROUP (4 X 4).

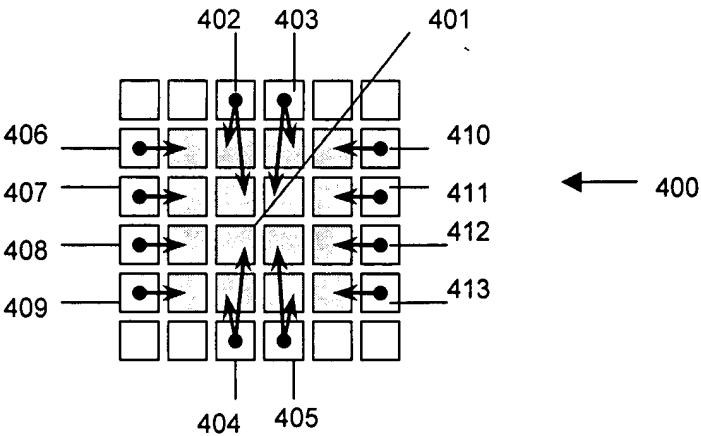


FIG. 6